

	Docum ent ID	U	Title	Current OR
1	US 59095 72 A	<input type="checkbox"/>	System and method for conditionally moving an operand from a source register to a destination register	712/226
2	US 57814 57 A	<input type="checkbox"/>	Merge/mask, rotate/shift, and boolean operations from two instruction sets executed in a vectored mux on a dual-ALU	708/231
3	US 56801 61 A	<input type="checkbox"/>	Method and apparatus for high speed graphics data compression	345/531
4	US 56253 74 A	<input type="checkbox"/>	Method for parallel interpolation of images	345/639
5	US 55944 37 A	<input type="checkbox"/>	Circuit and method of unpacking a serial bitstream	341/67
6	US 55792 53 A	<input type="checkbox"/>	Computer multiply instruction with a subresult selection option	708/625
7	US 54871 59 A	<input type="checkbox"/>	System for processing shift, mask, and merge operations in one instruction	712/223
8	US 54653 74 A	<input type="checkbox"/>	Processor for processing data string by byte-by-byte	711/219
9	US 54267 83 A	<input type="checkbox"/>	System for processing eight bytes or less by the move, pack and unpack instruction of the ESA/390 instruction set	712/225
10	US 54230 10 A	<input type="checkbox"/>	Structure and method for packing and unpacking a stream of N-bit data to and from a stream of N-bit data words	341/60
11	US 54086 70 A	<input type="checkbox"/>	Performing arithmetic in parallel on composite operands with packed multi-bit components	712/16
12	US 53901 35 A	<input type="checkbox"/>	Parallel shift and add circuit and method	708/518
13	US 52689 95 A	<input type="checkbox"/>	Method for executing graphics Z-compare and pixel merge instructions in a data processor	345/422
14	US 51876 79 A	<input type="checkbox"/>	Generalized 7/3 counters	708/706
15	US 51685 71 A	<input type="checkbox"/>	System for aligning bytes of variable multi-bytes length operand based on alu byte length and a number of unprocessed byte data	712/210
16	US 50954 57 A	<input type="checkbox"/>	Digital multiplier employing CMOS transistors	708/626
17	US 50816 98 A	<input type="checkbox"/>	Method and apparatus for graphics display data manipulation	345/422
18	US 49891 68 A	<input type="checkbox"/>	Multiplying unit in a computer system, capable of population counting	708/210
19	US 49032 28 A	<input type="checkbox"/>	Single cycle merge/logic unit	712/224
20	US 47713 79 A	<input type="checkbox"/>	Digital signal processor with parallel multipliers	712/42
21	US 47078 00 A	<input type="checkbox"/>	Adder/subtractor for variable length numbers	708/714
22	US 44981 77 A	<input type="checkbox"/>	M Out of N code checker circuit	714/806
23	US 44183 83 A	<input type="checkbox"/>	Data flow component for processor and microprocessor systems	710/307

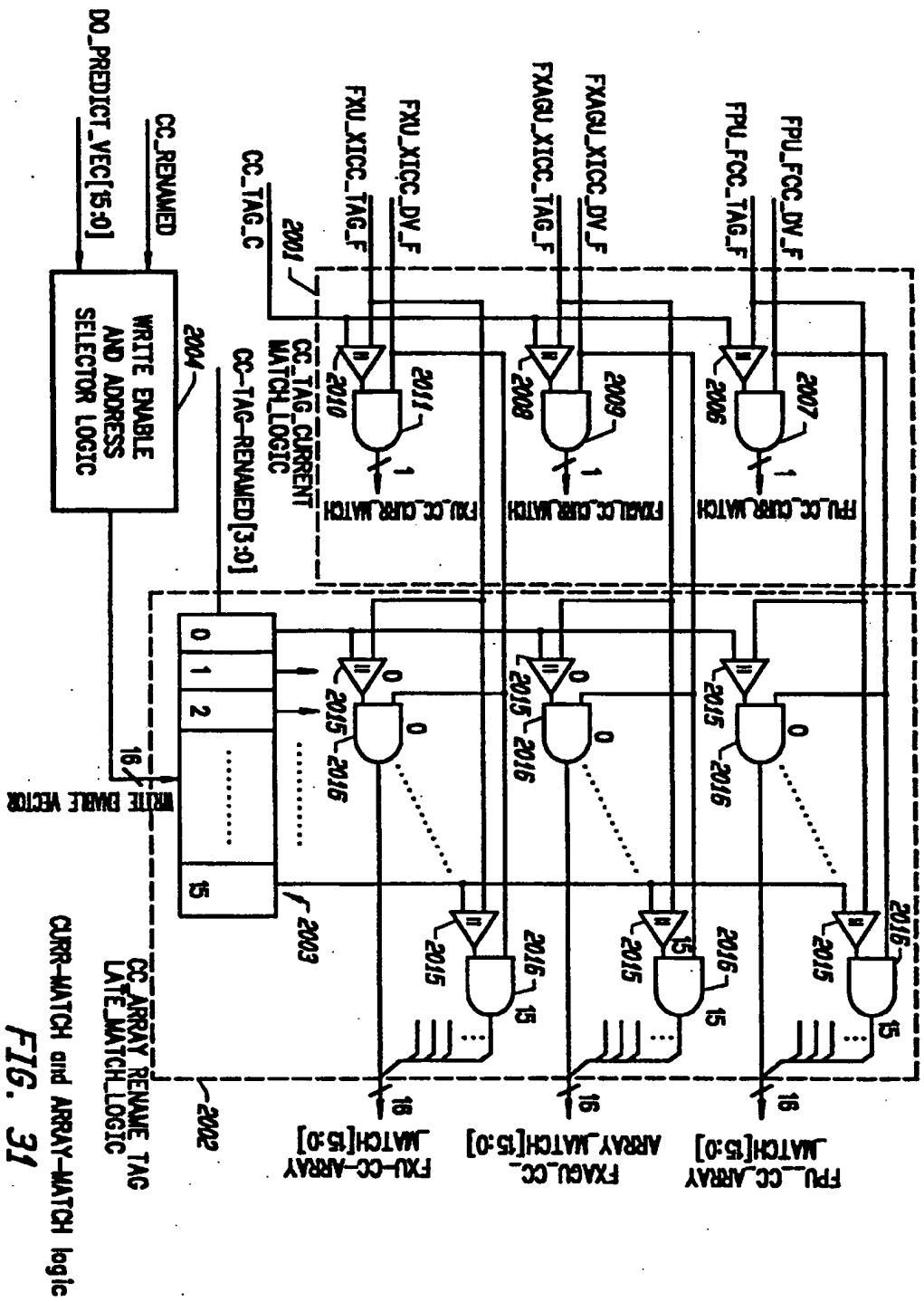


FIG. 31
CURR-MATCH and ARRAY-MATCH logic

	Docum ent ID	U	Title	Current OR
24	US 43934 68 A	<input type="checkbox"/>	Bit slice microprogrammable processor for signal processing applications	708/518
25	US 41617 84 A	<input type="checkbox"/>	Microprogrammable floating point arithmetic unit capable of performing arithmetic operations on long and short operands	708/513
26	US 41398 99 A	<input type="checkbox"/>	Shift network having a mask generator and a rotator	712/224
27	US 37237 15 A	<input type="checkbox"/>	FAST MODULO THRESHOLD OPERATOR BINARY ADDER FOR MULTI-NUMBER ADDITIONS	708/709
28	US 37116 92 A	<input type="checkbox"/>	DETERMINATION OF NUMBER OF ONES IN A DATA FIELD BY ADDITION	708/210

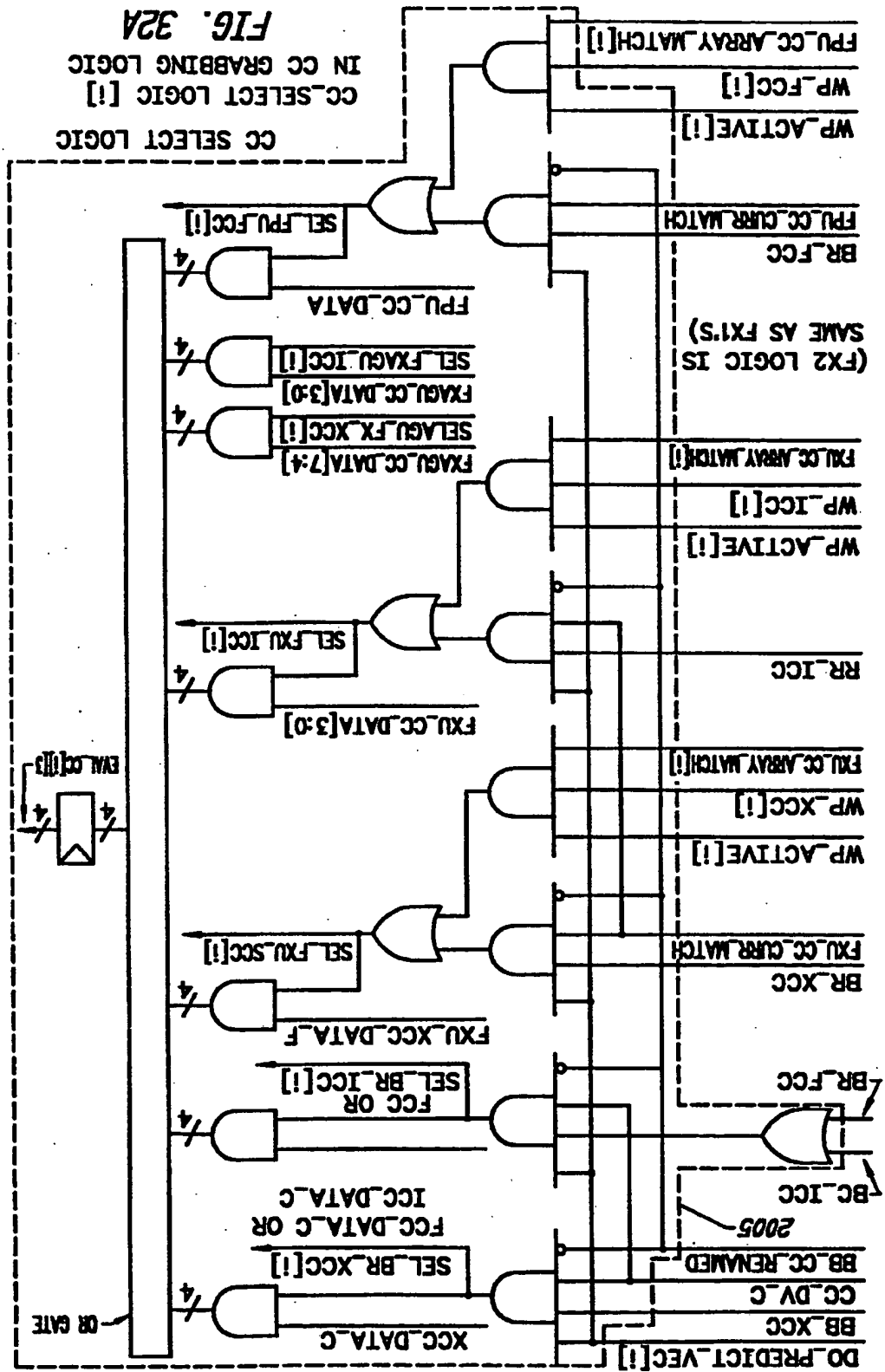


FIG. 32A
CC SELECT LOGIC
IN CC GRABBING LOGIC